These equations are true for any two-conductor system where the resistance of the conductors can be neglected and the medium between the conductors is well-behaved. These conditions are met by tracks on a printed circuit board for any track width which can be manufactured. The step which we have just described is a transverse electromagnetic disturbance. Since the equation relating current and voltage on a transmission line is $V = iZ_0$, it follows that the effect of a transmission line on the driving circuit can be considered in terms of a resistance $R = Z_0$ connected in place of the line. This was the procedure followed earlier in calculating the current drawn from the supply rail by a gate as it switches.

The impedance Z_0 depends on the cross-sectional geometry of the conductors employed and its calculation is extremely difficult except for very simple cases. It is, however, a relatively slowly varying function of the geometry[3] (usually logarithmic) and therefore this need not worry us too much. For a track on a printed circuit board laid out according to the design rules evolved in this paper a value of Z_0 of around 150Ω can be assumed.

One key feature of a board of logic which distinguishes it from most analogue systems is that there are a multiplicity of signal paths from various points scattered about the board to various other similar points. It is essential that each of these signal routes has an adjacent return path. The simplest way, conceptually, to achieve this is to provide a ground plane on one side of the board. In practice this is difficult since it usually requires multi-layer construction, with the increased cost and complexity which this entails, in order to accommodate the signal interconnexions. With Schottky t.t.l. it is not necessary to go to this extreme; all that is required is a ground grid laid out so that a signal line is never more than one inch away from its return path.

Ground loops. It might be argued that this scheme leads to ground loops which, from our experience with analogue systems (e.g. audio equipment) are to be avoided. The plain fact is though, that on a logic board, ground loops are of no importance. The reasons for this are somewhat complex but it is probably useful to note one simple argument. In a high-gain amplifier, induction of a few millivolts at the input due to ground loop pickup can lead to an output of the same order as the signal. In logic this is not the case; a few millivolts into a gate input make no difference whatsoever. Hundreds of millivolts of noise are required before we will significantly degrade the noise immunity of a t.t.l. system.

It is probably valuable to examine a situation where a logic board has been laid out in order to avoid ground loops. A possible layout of power and ground connexions, which is quite commonly adopted in the industry, is shown in Fig. 6. Now, if circuit A sends a step to circuit B there is no adjacent return path. In practice, since a fast step requires a return path it will simply use adjacent signal lines as returns, resulting in the induction of transient noise on these other signal lines. A further consequence is that the input to B will take a longer time to settle with a con-

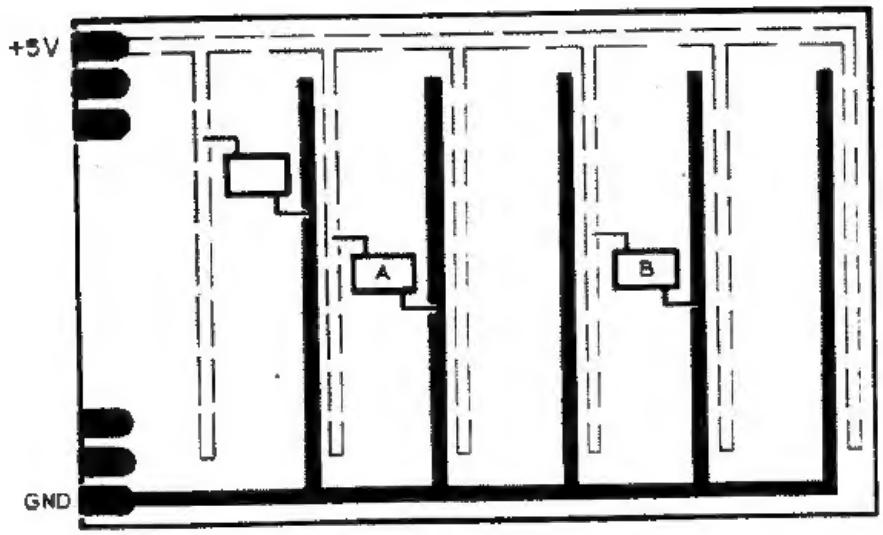

Fig. 6. A bad layout giving high inductance and few adjacent signal return paths, which leads to cross-talk.

sequent reduction in the speed of the system. As was explained earlier, the layout of Fig 6 is also bad from the point of view of placing excessive inductance in the way of charge travelling between i.cs and decoupling capacitors.

Recommended layout

A recommended scheme for laying out a printed circuit board is shown in Fig. 7. The power rails are run as close together as possible along the columns of integrated circuit packages and are interconnected at the top and bottom of the board. These provide return paths for logic signals travelling parallel to them. To provide return paths for signals travelling across the board the ground pins of the packages are connected together from left to right. Thin track, of the same thickness used for signal interconnexions can be used for this. A tantulum bead 10μF decoupling capacitor is provided between each pair of i.cs. Notice also that ground connexions are brought out at regular intervals across the edge connector. These provide return paths for signals travelling on and off the board.

If all these design rules are followed a reliable system will result and the consequent savings in servicing and testing will amply repay a little consideration given to board layout at the design stage.

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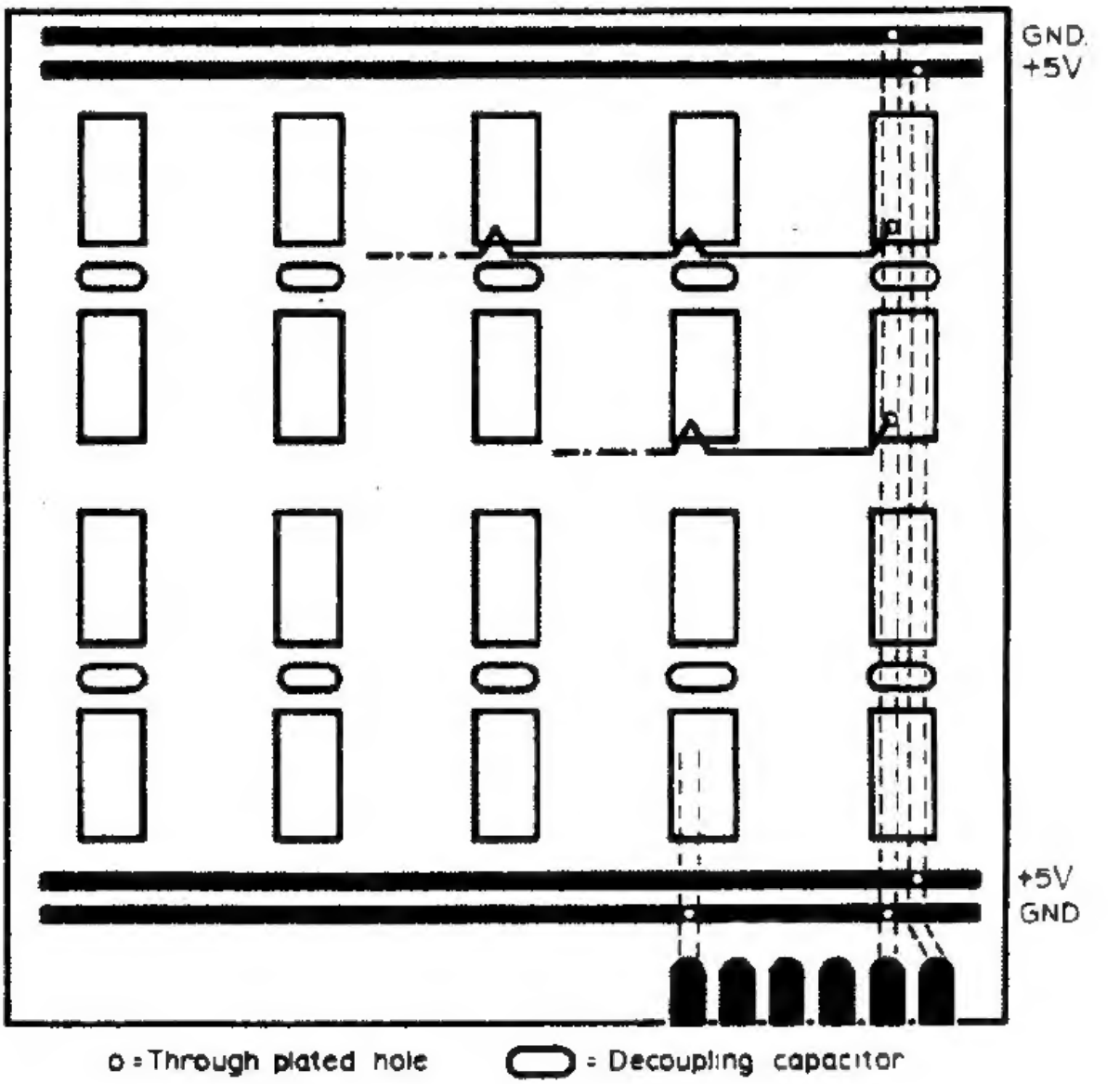

Fig. 7. Recommended layout.

DIGITAL ELECTRONICS LACKS SOUND THEORY

THE digital electronics industry has sprung up so quickly in the past ten years that the theoretical foundation required has not developed at all. It is impossible to cross the line separating the analogue and digital worlds. The sine wave is a periodic, time varying, steady state phenomenon, whereas a digital signal is a fixed amplitude step (shock wave). Each change of state is a single event in time and cannot be correlated with any other change. A dubious connection, via Fourier analysis, is merely a mathematical arpeggio, guaranteed to be worth a few exam questions at least. A leading edge of a step is a shock wave, it is a transverse electromagnetic wavefront which travels at the speed of light. Of course, it is possible to take this single step and analyse it using Fourier analysis, but this would mean combining an infinite number of sine waves which exist from minus infinity to plus infinity. This can be easily seen to be quite absurd and of no practical use.

The hard and fast rules laid down for periodic sine waves must be cast aside and new rules developed for the shock wave. An obvious area to concentrate on is signal distribution. We must have a basic understanding of the mechanism by which a block or pulse of energy is transmitted in space. This leads us into electromagnetic field theory and it is here that the student will learn and ultimately understand the subject of digital electronics.

Unfortunately, nearly all the books written on e.m. field theory are concerned with steady state sine waves. There is no basic theory written today which concentrates on high speed digital techniques. How 1ns steps propagate is known to only a few people. Yet with the advent of emitter coupled logic and Schottky t.t.l. this electrical phenomenon is becoming widespread. Engineers today attempt to put together fast, complex logic systems which stand the risk of failure. The paper design might well be satisfactory but the problems that arise during testing and commissioning seem endless. The unfortunate engineer just cannot understand the "gremlins" that keep upsetting his system. Nowhere is he taught the important fundamental principles necessary for competent digital system development.

To have a complete understanding of high speed systems one must apply certain techniques which are not taught in any educational establishment in the country, nor written about in any text book. One must go back to the turn of the century to find any suitable material. Then the main subject was telegraph signalling, which is analogous to digital transmission today. A 10-millisecond risetime step travelling 1,000 kilometres (telegraphy) is based upon the same theoretical principles as a 1-nanosecond step travelling 10 centimetres (computers).

Around 1890-1910 Oliver Heaviside and his contemporaries Lodge, S. P. Thompson, Hertz and Maxwell had developed many theories which should be used today. By thinking of digital signals as small, discrete packets of "energy current" flowing at the speed of light between the wires (which merely act as a guide) many of the present-day design implementation problems could be solved. The advent of the telephone and wireless led to the predominance of sinusoidal time varying signals, so the concept of "energy current" was lost as new theories were developed to cope only with the periodic waveform. We have now turned a full circle and must look backwards before we can advance.

The practical problems of digital systems, such as cross talk (noise), power supply decoupling, signal termination and drive techniques, component pulse response, earthing, and mains borne interference, need to be studied. General models and original concepts based upon Heaviside's "energy current" idea can be used to tackle these problems, making it possible to design complex digital systems in an orderly, scientific fashion. Every practising engineer in digital

electronics must stop attempting to use analogue ideas for digital systems: they will not work. Pattern sensitivity, noise, power supply problems are all raising their ugly heads, and all quite unnecessarily. By following clearly defined design rules, systems can be built which will work reliably and first time, without the usual 3-6 month commissioning troubles.

The design concepts that are used are not difficult. Although soundly based in theory, they do not involve exotic mathematics and are aimed specifically at practical problems of hardware development. They are tools of the trade to be used by all engineers and technicians.

Malcolm F. Davidson

DIGITAL ELECTRONICS THEORY

Mr Davidson's letter in the March issue contains so many sweeping statements and unjustified generalisations that one can only surmise that it was written to stimulate debate. Otherwise, why should someone having available "clearly defined design rules" and "certain techniques which are not taught in any educational establishment in the country, nor written about in any textbook" not share this privileged knowledge? Similarly one would have to conclude that Mr Davidson's knowledge of educational establishments and textbooks is significantly less universal than he implies. It would also seem that he has not heard of transmission line theory, nor of those of its areas which are particularly relevant to digital techniques, such as line driving and Bergeron diagrams. Further, he seems unaware of the connection between risetime-based (time domain) digital techniques and the corresponding Bode diagram (frequency domain) analogue methods, which is, for example, hinted in Mr Baxandall's article in the same issue.

No doubt other readers will be able to supply reading lists, including *Wireless World* articles, which should demonstrate that "the practical problems" have indeed been studied. I content myself with pointing out to Mr Davidson that within the Post Office engineers are aware of the problems, and courses are available for those who wish to be "taught the important fundamental principles for competent digital system development" including "how 1ns steps propagate".

T. M. Forcer
PO Marine Division
Southampton

DIGITAL ELECTRONICS THEORY

In reply to Mr Forcer (May Letters) my analysis of the digital electronics industry indeed contains "many sweeping statements" which at first glance do appear to be "unjustified". However, having spent over seven years in digital electronics it does not need much awareness on my part to see that the majority of engineers are incompetent at putting together fast logic. The industry is littered with complex computer systems that crash regularly, service engineers not knowing the reasons why. Too many students and engineers do not have a coherent set of design techniques to apply in their work.

In an attempt to rectify this catastrophic, myopic, situation I am working with two colleagues under the title of CAM Consultants and we regularly give seminars on digital techniques and we have written the first volume of a book on the subject to be published in May 1978.

The proof of the pudding is always in the eating and I ask Mr Forcer to name projects or systems which do not suffer from catastrophic failures from time to time. I must repeat that engineers today use analogue techniques (taught by the colleges) to solve digital problems, and thus they cannot solve them in a scientific fashion. For example, no company I have ever visited knows how to lay out a p.c.b. for high-speed logic applications. Because of this systems suffer from data dependent faults which one can only see by the failure of the system itself.

Finally, I would like to see any Post Office course notes on mains filters and power supply decoupling. Also I would be interested in hearing from other engineers who (mis)believe that digital electronics is based upon an adequate set of scientific principles and mathematical techniques, which lead to efficient reliable digital systems. If they exist show me!

Malcolm F. Davidson

DIGITAL ELECTRONICS THEORY

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Malcolm F. Davidson
CAM Consultants
South Mimms
Herts

INTERCONNECTION OF LOGIC ELEMENTS

The transmission line, T.T.L. and tri-state devices

By Catt, Davidson and Walton

This article outlines the concepts required when designing a complex logic system and describes the fundamental principles of connection between basic logic gates.

A digital system is composed of logic gates and interconnections between them. To ensure correct functioning of the system it is important to consider a model of this connection. The simplest case is a logic gate driving another single gate with no fanout as shown in Fig. 1. It is impossible to consider the interconnection without a ground or V_{cc} return path, and when this is present there is a distributed capacitance and inductance which forms a transmission line.

Properties of a transmission line

To characterise a transmission line a step propagating along a two-wire line is considered as shown in Fig. 2. Using Faraday's law of $V = d\phi/dt$ around loop abcd, L is defined as the inductance per unit length of the wire pair so $L = \phi/i$. In time t, the step will advance a distance s so that $s/t = c$ and the change of flux will be $\phi = L\,s\,i$. Substitution into Faraday's law gives the voltage applied to the line to overcome back e.m.f; $V_{AD} = L\,i\,ds/dt = L\,i\,c$. From $Q = VC$, $i = vCc$ where C is the capacitance per unit length of the wire pair, so $c = \pm 1/\sqrt{LC}$ and $v/i = Z_0 = \sqrt{L/C}$. Therefore, a step may propagate in either direction.

The two parameters which characterise a transmission line are the velocity of propagation c, and the impedance Z_0 which relates the voltage difference across the line to the current in the line. Thus, $v = iZ_0$ where Z_0 is a property of the geometry, and medium, μ and ϵ, in which the wires are embedded.

To use the formulae for Z_0 and c it is necessary to calculate L and C for any geometry that may be used. In general it is impossible to solve analytically for L and C and so other methods are used. Values for most practical cases are in the literature. It is common to represent a lossless transmission line as the model shown in Fig. 3 which allows the equations of step propagation to be derived. This method has little to recommend it especially as it appears to lead to a spurious high frequency cut-off. There is, of course, no high frequency cut-off inherent in any transmission line geometry and the only factor which can cause this is a frequency dependent behaviour of the dielectric. If the dielectric is vacuum, there is no frequency dependence and no cut-off.

The sinewave concept can be very misleading in digital electronics and it is invalid to think of a single step as being composed of a superposition of sine-

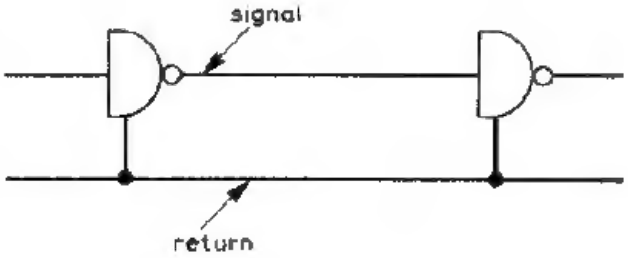
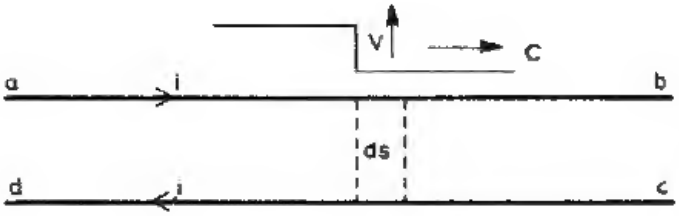


Fig 1. *Simple example of a logic gate driving another gate.*

Fig 2. *A step propagating along a two-wire line.*



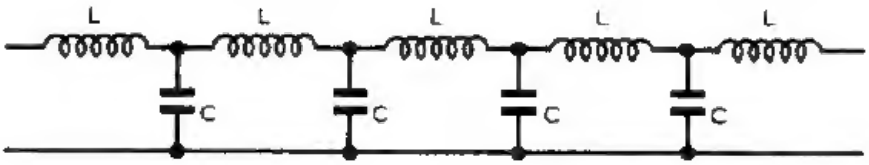
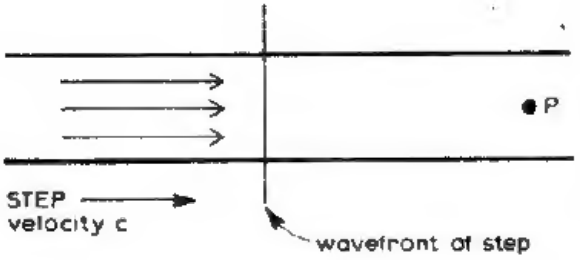


Fig 3. *Model of a lossless transmission line.*

Fig 4. *A simple step should not be considered as a superposition of sinewaves.*



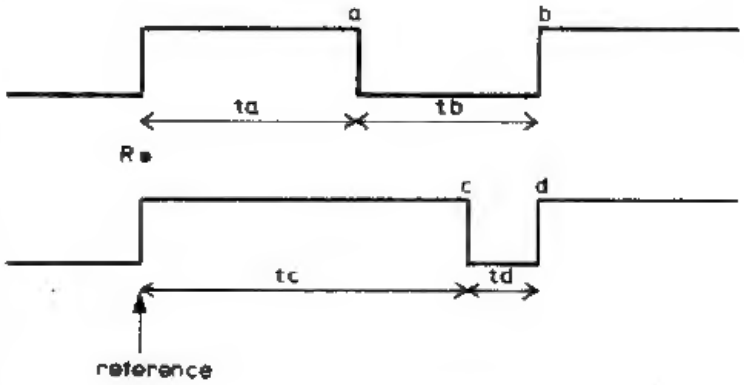


Fig 5. *Two digital signals, illustrating edges as separate events in time.*

waves. The diagram in Fig. 4 shows a step which is propagating along a transmission line with velocity c ($c = 1/\sqrt{\mu\epsilon}$), the velocity of light in the medium surrounding the conductors. A true sinewave signal is infinite in both time and distance, i.e: it can only exist in an infinitely long transmission line, and any practical situation is an approximation to this ideal. Because the step is travelling at the velocity of light there can be no energy or information ahead of it and there can be no effect at any point P in front of the step. This consideration alone is sufficient to demonstrate that such a step cannot be analysed into a superposition of sinewaves because these sinewaves would have to exist both ahead of and behind the step. Also, if the transmission lines were cut before the step arrived at P, any effect which was already at P would have to vanish instantaneously, again impossible. Mathematics indicate that if we superpose many sinewaves of appropriate amplitudes and phase relationships we would obtain a step waveform. This is undeniably true but its converse, that we can analyse a step into a superposition of sinewaves, does not follow logically and is in fact not true. The sinewave is responsible for much confusion particularly in the discussion of factors affecting the choice of capacitors for logic decoupling. It is important to remember that a step is a shock wave, formed by a transverse electromagnetic wave front travelling at the speed of light, and all digital signals are combinations of either positive or negative going edges. Any observer can only see the signal as it passes him on the transmission line.

The important parameter of the two digital signals in Fig. 5 is the time delay between the edges. Each edge a, b, c or d must be considered as a separate event in time which is completely unconnected with any other transition. A logic gate connot predict the arrival of any edge until the shock wave actually arrives. It then responds to the amplitude of the signal and by the time the next shock wave arrives it has settled down to the steady state condition.

Transistor transistor logic

Before discussing t.t.l. circuits it is worth considering the evolutionary process which lead up to them. In early d.t.l., transistors were only capable of sustaining a 1mA collector current which resulted in the circuit arrangement shown in Fig. 6 where a 10kΩ resistor was used in the collector. One problem with this circuit is its inability to drive stray capacitance. Consider the output waveform in Fig. 7 which is obtained when a pulse is applied to the input. The transistor switches on and the stray capacitance is discharged through the saturated transistor to produce a rapid falling edge. When the transistor switches off it cannot supply current so the stray capacitance charges through the 10kΩ resistor to produce an exponential rise which corresponds to a time constant of RC. Therefore, this type of gate is not very good at driving long signal lines. In practice the load is not strictly capacitive, but is a transmission line with a characteristic impedance of around 100Ω. However, in this case because R is much greater than 100Ω it makes very little difference and the slow edge masks any transmission line effects.

Logic designers attempted to circumvent this problem by using a "push-

pull" output stage to give rapid transitions in both directions as shown in Fig. 8. Here the output is driven by a "phase splitter" so that while the top transistor is on the bottom one is off and vice versa, but in practice there is an overlap of a few ns. This causes a low impedance across the supply rails which produces a current spike. This type of output was used in the unpopular 73 series of logic. The final step in the evolution of t.t.l. was the insertion of a series limiting resistor in the collector of the upper transistor.

Unfortunately, during the evolution of t.t.l the way impedance levels and device speeds have changed has not been considered fully. While d.t.l. worked initially with a 10kΩ output impedance we now have t.t.l. devices with an internal pull-up resistor of around 100Ω. This means that the transmission line behaviour cannot now be ignored. In fact, when the connection to a t.t.l. device is considered as a transmission line the upper transistor in the output is redundant and serves no useful purpose. A capacitive load requires a circuit as shown in Fig. 9 because, to produce a voltage across the capacitor, a charge must be fed into it via S_1. Discharge of the capacitor must take place through S_2. As already mentioned, a t.t.l. gate must drive a transmission line with an impedance of about 100Ω. The current and voltage are related by $V = iZ_o$ where V is the voltage applied to the line and i is the resulting current. In this case the load is essentially resistive and only one switch is required as shown in Fig. 10. When S is closed the output is low and when it is open the output is high. If the interconnection is terminated with a resistor $R = Z_o$, effects due to stray capacitance and inductance will not affect the output rise or fall times. Therefore, under certain conditions the t.t.l. "push-pull" configuration is unnecessary and an open collector gate will suffice.

Tri-state devices

Common data-bus structures are widely used in mini computer systems but because conventional t.t.l. cannot be wire-ORed it cannot be used. To overcome this limitation tri-state devices have been produced and are rapidly becoming standard components for bus drivers and memory outputs. A tri-state device has an additional control input which determines whether or not the device is enabled. When enabled, its outputs are in the high or low states as normal. When disabled, its outputs assume the high-impedance or off state and the device behaves almost as though its outputs are disconnected from the package pins. In this system only the device which is driving the bus is enabled, so active pull-up is achieved with the benefits of wire ORing. However, even with these apparent advantages it must be considered whether tri-state t.t.l. is necessary and desirable.

With regard to its necessity, the answer is definitely no. Any function which is possible with tri-state devices can be implemented more simply with open-collector t.t.l. Tri-state is an unfortunate development caused by a misunderstanding of the requirements for transmission line driving. The answer is also no for desirability because it has a failure mode which can lead to the progressive collapse of all the tri-state devices driving a bus. For example, in Fig. 11 if device A becomes enabled at the wrong time due to a fault

in the circuitry it could place all lows on a bus to which another device is quite legitimately outputting all highs. This leads to catastrophic power dissipation in the good device and the process can then repeat until all of the devices are destroyed. For the TI 74365 hex bus-driver, power dissipation in this failure mode can be calculated as follows. The output short-circuit current is specified as 40-130mA so the power dissipation per gate for a 5V rail will be between 0.2 and 0.65W, and the total dissipation for a package of six gates will be 1.2 to 3.9W. The quiescent power dissipation of 0.3 to 0.4W per package means that the total worst case figure is 4.3W. This is about ten times the rated dissipation of a d.i.p. and will destroy the device. □

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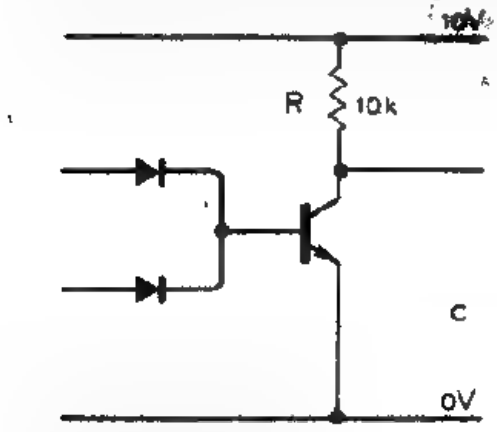

Fig 6. *Early form of logic, diode-transistor logic.*

Fig 7. *Output waveform from d.t.l. in Fig 6.*

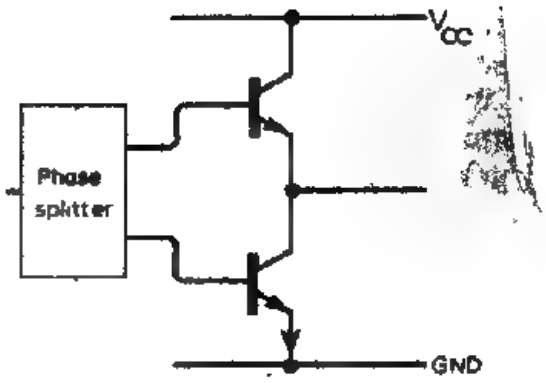

Fig 8. *Push-pull output stage to give rapid transitions.*

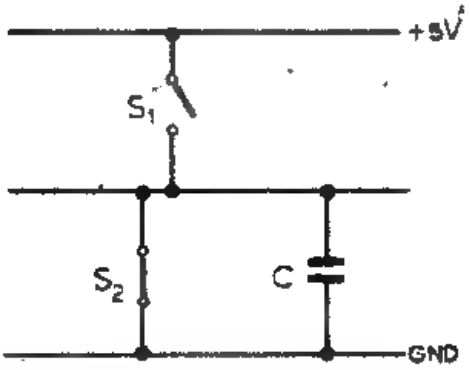

Fig 9. *Basis of t.t.l. circuit required to drive a capacitive load.*

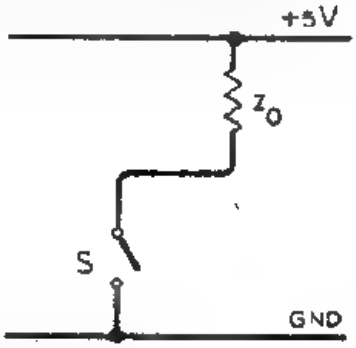

Fig 10. *Only one switch required for a resistive load.*

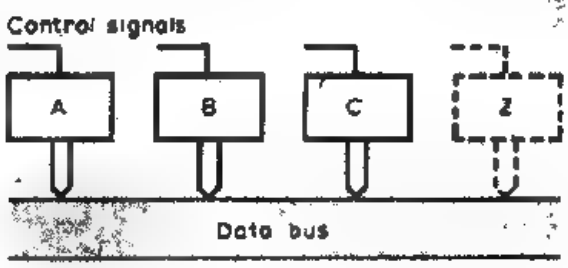

Fig 11. *Tri-state devices connected to a bus.*

C.A.M.

Mains interference and filtering

Protecting logic systems from mains borne noise

by **I. Catt and M. F. Davidson** (CAM Consultants), and **D. S. Walton** (Icthus Instruments Limited)

Although great trouble is taken when designing d c power supplies for large digital systems interference on the mains power lines is often overlooked or underestimated. This article outlines the types of noise that occur, and describes a suitable filter for overcoming the problem

INTERFERENCE from the mains can be classified into three types. Balanced, where the noise signal travels equally down the live and neutral lines, and the earth line acts as a return path. This is often called common mode noise, and it causes earth currents which can upset high gain linear circuits. Unbalanced, where the noise signal travels down the live line and back on the neutral line, leaving the earth line unaffected. This is often called differential mode noise and may be lost or suppressed in the d.c. power supplies of a circuit. It can be shown that any complex signal travelling down the three lines can be resolved into a common mode component and a differential mode component. Mains borne radiated noise, which can be both balanced and unbalanced, enters the equipment via the three power lines, and then radiates directly into the logic.

Susceptibility of a digital system to mains noise

Differential mode noise on the live and neutral lines tends to be smoothed out at the unregulated and regulated d.c. points. However, because large value capacitors have a significant series inductance, some of the noise, if not suppressed before the transformer primary, will pass through the power supply and cause transient variations which can disrupt the logic operation. Screening the transformer will not help significantly because differential noise is fed through the transformer from primary to secondary and not via inter-winding capacitance.

Common mode noise, however, does pass through the transformer via inter-winding capacitance, so a screened transformer will help to suppress the interference. The typical inter-winding capacitance for an unscreened transformer is 100pF. With screening, this falls to around 1pF. Any common mode noise that does pass through the transformer tends to raise the positive voltage relative to 0V, and tends to lift the level of 0V at some points but not others. The use of a choke rather than a link between 0V and earth will help to render the logic immune to this noise

because all of the logic supply lines will tend to move together. Therefore, any common mode noise which does pass through the regulated d.c. supply will see three loads in series. The link between the earth line and frame, the link between frame and 0V, and the line carrying 0V across the logic to the link. If the 0V to frame to earth link has a high impedance, such as a choke, most of the noise will appear harmlessly across it. The d.c. resistance of the choke should be below 0.1Ω to conform to BS3861. If, however, the 0V to earth link is a low impedance, the noise will lift the potential at one point on the 0V grid. This will degrade the logic signals and tend to cause a malfunction.

Mains borne radiated noise, which is emitted from the mains wiring, can be greatly reduced by screening the live and neutral lines, and earthing the screens to the frame. Another method of reducing the radiated noise is to include a mains filter at the point where the power lines enter the circuit module. A third approach is to have mains lines in the module separated from the vulnerable logic by correctly earthed bulkheads. Once past the mains filter, the mains cables do not normally need to be screened. If power is switched on and off to loads within the module these power lines should also be screened.

Magnitude of mains borne interference

A reasonable noise amplitude to design against in a 240V single phase supply is 2kV over the range 100kHz to 10MHz. The noise may be common mode or differential mode and can be caused by, for example, switching off an electric motor which is on the same supply. It is wise to assume large amplitude noise above the nominal 240V of the line, and also that it is both common and differential mode.

The source impedance of the noise is difficult to determine, but it is safest to assume a very low source impedance of, say, two ohms. Both of these assumptions might surprise the reader, but they have been chosen to give a reasonable safety margin.

Mains filtering

Mains filters are constructed from capacitors and inductors. The capacitors require an adequate voltage rating and also have to be able to dissipate the heat generated from the maximum current. By Ohm's law, $V = I Z$ so $I = V/1/6\ fC$ which is 240 . 300 . C. Therefore, for a 1fiF capacitor the current is around 100mA. It is worth noting that the mains filter can significantly alter the power factor of a load. The series inductance of such a capacitor can be as low as 10nH, which is very satisfactory in this application.

With inductors, it is important to make sure that they do not saturate at the peak current. If the power taken by a circuit is around 1kW, the r.m.s. current is around 4A and the peak current may be as high as 10A. A choke which saturates at 20A and has an inductance of 200μH can have a parallel capacitance as low as 10pF which again is satisfactory for this application. The d.c. resistance of such a choke is around 0.1 ohms, so it is possible to meet the safety requirements even if the choke is placed in the earth line.

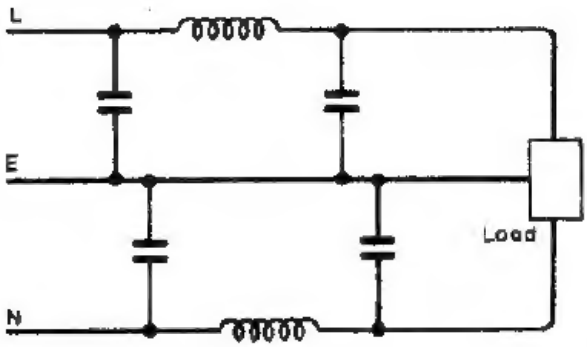

Fig. 1

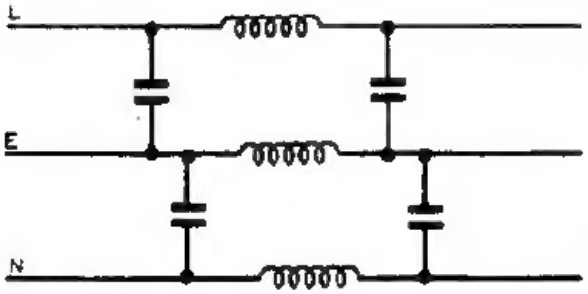

Fig. 2

A mains filter is a low pass device and the usual circuit is a double π as shown in Fig. 1. High frequency signals entering either the live or neutral lines see a high impedance inductor ahead and are shunted to earth through a low impedance capacitor. Typically, at 1MHz, with 1μF capacitors and 200μH inductors, Z_c is around 0.2Ω and Z_L is around 1kΩ. If the source impedance of the noise is 1kΩ or higher, the noise is attenuated by a factor of 1kΩ/0.2Ω = 5,000 or about 70dB. If the source impedance of the noise is low, the first capacitor is ineffective, but the potential divider formed by the inductor and the second capacitor still gives around 70dB attenuation at 1MHz.

Any high frequency signals approaching from either direction see a short to earth, and a high impedance series inductor blocking the path ahead. This arrangement works well if noise is the only problem. But, because the input and output of both lines are connected together at high frequency, an "earth loop" pickup of externally radiated noise can occur. Also, the possibility of electrostatic discharge into the circuit is much more likely. From the point of view of radiated noise the circuit in Fig. 2, which blocks the passage of high frequency signals down all of the lines, is preferable. It makes the path down the lines an open circuit to high frequencies, and tends to isolate the system. This filter does however cause a disquieting amount of earth current. If the capacitors are 1μF, the total earth current is about 150mA. With the circuit rearranged as in Fig. 3, the noise suppression is virtually unaltered and the earth current is reduced to around 2mA. This circuit is also safer because there are no components linking live directly to earth, and a single shorted capacitor does not present a safety hazard. The two resistors discharge the capacitors if the filter is disconnected from the mains.

Commercial mains filters

Medium performance commercial filters have a specification of around 60dB insertion loss in the region of 1MHz. A filter of this type would cause 2kV of noise to be reduced to a mere 2V, which would easily be suppressed on its way through the power supply. Higher performance filters, specified at 100dB insertion loss, reduce noise of 2kV down to an unnecessarily low 20mV. The most serious shortcoming in commercial units is when the windings of both

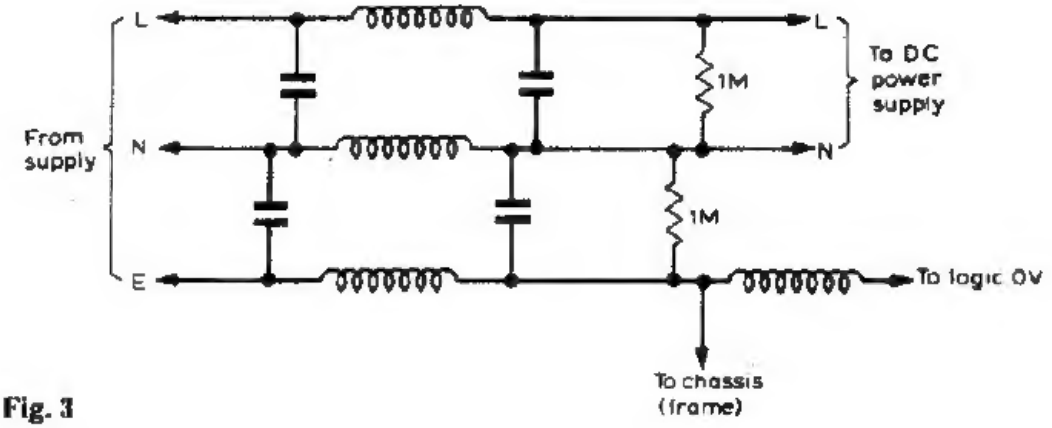

Fig. 3

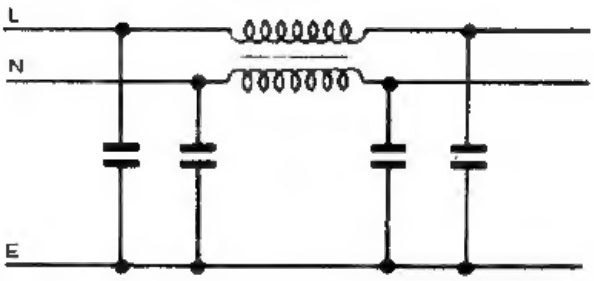

Fig. 4

chokes are on the same core as shown in Fig. 4. The theory is that the currents in the live and neutral lines, being equal and opposite, create zero total magnetic flux in the choke. This means that for a heavy live and neutral current the core will not saturate, and a single toroid can be used in place of two separate and more expensive chokes. However, instead of two chokes there is a transformer which will not stop any differential mode noise. The author has not seen a manufacturer's specification where insertion losses for both differential and common mode noise have been unambiguously defined. The insertion loss is the ratio of the output amplitude from the filter into a load divided by the input from a source with the same impedance. Sometimes the specification does not state this impedance so it is virtually impossible to determine the filter performance. The correct specification is the minimum insertion loss when the source impedance and load impedance are independently varied from zero ohms to open circuit. □

TRI-STATE DEVICES IN LOGIC SYSTEMS

Messrs. Catt, Davidson and Walton in "Interconnections of Logic Elements" (June issue, page 62) made the following statement: "Any function which is possible with tri-state devices can be more easily implemented with open collector t.t.l. Tri-state is an unfortunate development caused by the misunderstanding of the requirements for transmission line driving."

By definition open collector devices require a collector load which would take the form of resistors on the bus, introducing more components, and more complexity. Catastrophic power dissipation caused by progressive collapse of tri-state devices is only partially relevant as most m.o.s. devices have current limited outputs preventing such failure. Surely all the design engineers of bus orientated microprocessors by Motorola, Intel, Texas, Zilog, etc., could not have misunderstood line driving requirements?

B. A. Hutchinson
Department of Electrical & Electronic Engineering
University of Newcastle upon Tyne

The authors reply:

Mr Hutchinson quotes two sentences from the article in which the following statements are made:

1. Open collector t.t.l. is a superior replacement for tri-state t.t.l. in all applications in which the latter is used.
2. Tri-state t.t.l. is an unfortunate development.
3. Tri-state t.t.l. is a product of the same wrong-thinking which originally led to t.t.l., viz. a basic misunderstanding of how to model the interconnection between logic gates.

Mr Hutchinson appears to be taking issue with (1) and (2) but he gives no reasoned argument for dismissing the discussion leading to (3).

His objection to (1) seems to be based on the assertion that tri-state t.t.l. requires considerably more components to implement a particular bus arrangement because of pull-up resistors. This argument is presumably based on the idea that each open-collector gate requires its own pull-up resistor. This is not so. Pull-ups are only required at each end of the bus connections (i.e. two places) where they serve as terminations matched to the characteristic impedance of the bus lines. These resistors would normally take the form of d.i.ps and hence represent small overhead in terms of cost, failure modes, etc.

Mr Hutchinson goes on to discuss protection of m.o.s. tri-state outputs against catastrophic failure. He may be correct. Our article, however, is concerned with t.t.l. and its variants and it was not our intention to make any assertions concerning m.o.s., this would require a separate article. In the case of tri-state t.t.l., I have two communications from semiconductor manufacturers stating that the failure mode we described does exist.

His final argument, a variation on the theme of "So many people cannot be wrong," hardly requires an answer. Fortunately correctness or incorrectness is based, not on a democratic consensus, but on reasoned argument and experiment. We are prepared to demonstrate the validity of our conclusions before any scientific or engineering audience which Mr Hutchinson cares to assemble.

I. Catt, M. F. Davidson and D. S. Walton